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FEE TRANSMITTAL for FY 2006

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	620.00

Complete if Known	
Application Number	09/981,620
Filing Date	October 16, 2001
First Named Inventor	Richard Coulson
Examiner Name	K. Verbrugge
Art Unit	2188
Attorney Docket No.	42390P11456

METHOD OF PAYMENT *(check all that apply)*

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FEE CALCULATION

Large Entity		Small Entity			
Fee Code	Fee ($)	Fee Code	Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	120.00
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) ____

SUBTOTAL (2) ($) 620.00

SUBMITTED BY — Complete (if applicable)

Name (Print/Type)	Mark C. Van Ness	Registration No. (Attorney/Agent)	39,865	Telephone	(503) 439-8778
Signature				Date	12/29/06

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wr) 12/15/2004.
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Matthew C. Fagan
INTEL AMERICAS, INC.
1501 S Mo Pac Expy Ste 400
MS AN1-PTL1
Austin TX 78746-7544
Phone: (512) 732-3936
Fax: (512) 732-3912

Fax

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IN RE THE APPLICATION OF:	Richard L. Coulson	CONFIRMATION NO.:	6345
APPLICATION NO.:	09/981,620	ART UNIT:	2189
FILED:	October 16, 2001	EXAMINER:	Kevin Verbrugge
TITLE:	NON-VOLATILE CACHE TO REDUCE POWER CONSUMPTION (AS PREVIOUSLY AMENDED)		
ASSIGNEE:	INTEL CORPORATION		

Enclosed are the following:
This Facsimile Cover Sheet - 1 page
Transmittal Form - 1 page
Fee Transmittal - 1 page (in duplicate)
Appeal Brief - 17 pages

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Application Number	09/981,620
Filing Date	October 16, 2001
First Named Inventor	Richard L. Coulson
Art Unit	2189
Examiner Name	Kevin Verbrugge
Attorney Docket Number	42390P11456
Total Number of Pages in This Submission	

ENCLOSURES (Check all that apply)

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
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- [ ] Information Disclosure Statement
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- [ ] Drawing(s)
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- [ ] Proprietary Information
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name			
Signature	/Matthew C. Fagan, Reg. No. 37,542/		
Printed name	Matthew C. Fagan		
Date	December 31, 2006	Reg. No.	37,542

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ATTORNEY'S DOCKET NO. <u>42390P11456</u> *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE THE APPLICATION OF:	Richard L. Coulson	CONFIRMATION NO.:	6345
APPLICATION NO.:	09/981,620	ART UNIT:	2189
FILED:	October 16, 2001	EXAMINER:	Kevin Verbrugge
TITLE:	NON-VOLATILE CACHE TO REDUCE POWER CONSUMPTION (AS PREVIOUSLY AMENDED)		
ASSIGNEE:	INTEL CORPORATION		

APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Appellant respectfully submits this Appeal Brief following the Notice of Appeal filed October 17, 2006.

Appellant respectfully petitions for a one month extension of time to extend the period to submit this Appeal Brief to January 17, 2007.

I, Matthew C. Fagan, Reg. No. 37,542, hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office on December 31, 2006.

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02 FC:1402 500.00 DA

i. *Real Party in Interest*

Intel Corporation, a Delaware corporation.

ii. *Related Appeals and Interferences*

None.

iii. *Status of Claims*

Claims 1-106, 108, 127, and 138 are canceled.

Claims 107, 109-126, 128-137, and 139-148 are rejected.

Claims 107, 109-126, 128-137, and 139-148 are on appeal.

iv. *Status of Amendments*

No amendment has been filed subsequent to final rejection.

v. *Summary of Claimed Subject Matter on Appeal*

Features of independent claims 107, 126, and 137 cover, without limitation, one or more example embodiments shown in the drawings and described in the Detailed Description of Applicant's application as indicated in parentheses.

Independent claim 107

Independent claim 107 recites an apparatus comprising:

non-volatile cache memory (e.g., non-volatile cache memory 14 of Fig. 1); and

a controller (e.g., memory control 16 of Fig. 1) to control access to a rotating storage device (e.g., disk memory 12 of Fig. 1) in response to requests, the controller to spin down the rotating storage device (e.g., p. 4 at l. 23; p. 8 at ll. 21-26), to queue one or more operations for the rotating storage device (e.g., block 56 of Fig. 4; p. 5 at ll. 18-19; p. 6 at ll. 15-19 and 23-25; p. 7 at ll. 16-18, 20-21, and 24-25; p. 8 at ll. 11-13), to spin up the rotating storage device to perform a read operation for a read request in response to a miss in non-volatile cache memory for the read request (e.g., blocks 26 and 28 of Figs. 2-3; blocks 32 and 34 of Fig. 3; p. 4 at ll. 22-

24; p. 5 at ll. 10-17), and to perform one or more queued operations for the rotating storage device in response to the miss (e.g., block 30 of Figs. 2-3; p. 4 at ll. 24-25; p. 5 at ll. 18-21),

wherein the controller is to queue one or more operations for the rotating storage device while the rotating storage device is spun down (e.g., block 24 before block 26 in Fig. 2; p. 4 at ll. 16-23; p. 5 at ll. 5-8 and 18-19; p. 6 at ll. 22-25; p. 7 at ll. 16-18; p. 8 at ll. 11-13 and 24-26).

Independent claim 126

Independent claim 126 recites a method comprising:

spinning down a rotating storage device (e.g., disk memory 12 of Fig. 1; p. 4 at l. 23; p. 8 at ll. 21-26);

queuing one or more operations for the rotating storage device (e.g., block 56 of Fig. 4; p. 5 at ll. 18-19; p. 6 at ll. 15-19 and 23-25; p. 7 at ll. 16-18, 20-21, and 24-25; p. 8 at ll. 11-13), wherein queuing one or more operations for the rotating storage device comprises queuing one or more operations while the rotating storage device is spun down (e.g., block 24 before block 26 in Fig. 2; p. 4 at ll. 16-23; p. 5 at ll. 5-8 and 18-19; p. 6 at ll. 22-25; p. 7 at ll. 16-18; p. 8 at ll. 11-13 and 24-26); and

in response to a miss in non-volatile cache memory (e.g., non-volatile cache memory 14 of Fig. 1) for a read request, spinning up the rotating storage device and performing a read operation for the read request and one or more queued operations for the rotating storage device (e.g., blocks 26, 28, and 30 of Figs. 2-3; blocks 32 and 34 of Fig. 3; p. 4 at ll. 22-25; p. 5 at ll. 10-17 and ll. 18-21).

Independent claim 137

Independent claim 137 recites a system comprising:

a hard disk drive (e.g., disk memory 12 of Fig. 1; p. 2 at ll. 22-23; p. 8 at l. 21);

non-volatile cache memory (e.g., non-volatile cache memory 14 of Fig. 1); and

a controller (e.g., memory control 16 of Fig. 1) to control access to the hard disk drive in response to requests, the controller to spin down the hard disk drive (e.g., p. 4 at l. 23; p. 8 at ll. 21-26), to queue one or more disk operations (e.g., block 56 of Fig. 4; p. 5 at ll. 18-19; p. 6 at ll. 15-19 and 23-25; p. 7 at ll. 16-18, 20-21, and 24-25; p. 8 at ll. 11-13), to spin up the hard disk drive to perform a disk read operation for a read request in response to a miss in non-volatile

cache memory for the read request (e.g., blocks 26 and 28 of Figs. 2-3; blocks 32 and 34 of Fig. 3; p. 4 at ll. 22-24; p. 5 at ll. 10-17), and to perform one or more queued disk operations in response to the miss (e.g., block 30 of Figs. 2-3; p. 4 at ll. 24-25; p. 5 at ll. 18-21),

wherein the controller is to queue one or more disk operations while the hard disk drive is spun down (e.g., block 24 before block 26 in Fig. 2; p. 4 at ll. 16-23; p. 5 at ll. 5-8 and 18-19; p. 6 at ll. 22-25; p. 7 at ll. 16-18; p. 8 at ll. 11-13 and 24-26).

vi. *Grounds of Rejection to be Reviewed on Appeal*

1. Whether claims 107, 109-110, 115, 118, 122-126, 128-129, 134, 137, 139-140, 145, and 148 are anticipated under 35 U.S.C. § 102(b) by UK Patent Application GB 2 286 267 A to Cohn et al. ("Cohn").

2. Whether claims 111-114, 119-121, 130-133, and 141-144 are unpatentable under 35 U.S.C. § 103(a) over Cohn.

3. Whether claims 116-117, 135-136, and 146-147 are unpatentable under 35 U.S.C. § 103(a) over Cohn in view of IBM Technical Disclosure Bulletin NN9411421 ("TDB").

vii. *Argument*

1. **Whether claims 107, 109-110, 115, 118, 122-126, 128-129, 134, 137, 139-140, 145, and 148 are anticipated under § 102(b) by Cohn.**

Claims 107, 126, and 137

Independent claims 107 and 126 refer to queuing one or more operations for a rotating storage device while the rotating storage device is spun down.

Independent claim 137 refers to queuing one or more disk operations while a hard disk drive is spun down.

Applicant respectfully submits Cohn did not teach or suggest such feature(s) as claimed.

Cohn taught that sectors of data that are written to cache memory 106 of Figure 1 are designated in cache memory 106 as being in a New state. A sector in any state in cache memory 106 may be overwritten with new data for the same sector and designated as New. A sector in an Invalid or Consistent state in cache memory 106 may be replaced or overwritten with data for a

different sector which is then designated as New. See, e.g., p. 7 at ll. 4-12; p. 11 at l. 33 to p. 12 at l. 2; p. 12 at ll. 5-7; p. 13 at l. 31 to p. 14 at l. 2.

Cohn also taught that a sector in cache memory 106 remains in the New state until the sector is destaged, that is transferred, to update disk 104. The sector in cache memory 106 is then designated as Consistent, allowing the sector to be replaced. See, e.g., p. 7 at ll. 4-12; p. 10 at ll. 33-35; p. 11 at ll. 1-3 and ll. 29-32.

Cohn taught that destaging is not performed until disk 104 is required to be accessed due to a read cache miss, a large read, or a large write to satisfy a request. This is to reduce the number of times that disk 104 has to be activated, that is accelerated to operating speed, to reduce power consumption. See, e.g., p. 2 at ll. 13-19; p. 11 at ll. 1-2 and 17-19; p. 12 at l. 15 to p. 13 at l. 2; p. 14 at ll. 11-14.

Cohn also taught that destaging is performed by arranging sectors in the New state in cache memory 106 into a particular Destaging Order and then transferring such sectors from cache memory 106 to disk 104 in the Destaging Order. See, e.g., p. 11 at ll. 10-16.

The July 17, 2006 Final Office Action ("Final Office Action") on page 8 at line 15 through page 9 at line 6 appears to equate Cohn's designating sectors as New in cache memory 106 with queuing operations for a rotating storage device (claims 107 and 126) and with queuing disk operations (claim 137) as claimed by Applicant.

Applicant respectfully submits, however, that a designated state of a sector in cache memory 106 cannot be equated with an operation. Simply put, a status is not an operation. Applicant respectfully submits that a New state designation for a sector in cache memory 106 does not direct control system 108 of Cohn to do anything. Rather, Cohn taught that it is a destaging operation which directs writing New sectors from cache memory 106 to disk 104. See, e.g., p. 11 at ll. 10-16. Applicant also respectfully submits that a sector designated as New in cache memory 106 similarly cannot be equated with an operation.

Even assuming arguendo that a status or a sector designated with a status could somehow be equated with an operation, Applicant also respectfully submits that Cohn did not teach any queuing of New states or queuing of New sectors while disk 104 is spun down. Applicant respectfully submits the term queue and its derivatives connote order. Cohn, however, taught

that any sectors designated as New are ordered when destaging occurs. See, e.g., p. 11 at ll. 10-16. Applicant therefore respectfully submits that Cohn did not teach any queuing of New states or queuing of New sectors when sectors in cache memory 106 are being designated as New while disk 104 is spun down.

Applicant also respectfully submits that the arranging of sectors in a Destaging Order as taught by Cohn cannot be equated with queuing any operations while a rotating storage device (claims 107 and 126) or a hard disk drive (claim 137) is spun down, as claimed by Applicant. Cohn taught that destaging is restricted to occasions when disk 104 is required to be accessed for a request that cannot be satisfied from cache memory 106. See, e.g., p. 2 at ll. 13-19. Cohn also taught that destaging is performed only when disk 104 is spinning. See, e.g., Cohn on page 11 at lines 1-2. Applicant therefore respectfully submits that the arranging of sectors in a Destaging Order in Cohn does not occur while disk 104 is spun down.

For at least the above reasons, Applicant respectfully submits claims 107, 126, and 137 are not anticipated by Cohn.

Claims 109-110, 115, 118, 122-125, 128-129, 134, 139-140, 145, and 148

Noting claims 109-110, 115, 118, 122-125, 128-129, 134, 139-140, 145, and 148 depend from independent claim 107, 126, or 137, Applicant respectfully submits these claims are also not anticipated by Cohn.

2. **Whether claims 111-114, 119-121, 130-133, and 141-144 are unpatentable under § 103(a) over Cohn.**

Claims 111 and 141

Claims 111 and 141 depend from independent claims 107 and 137, respectively, and refer to queued operation(s) comprising a prefetch operation.

Applicant respectfully submits Cohn did not teach or suggest such feature(s) as claimed.

Applicant also respectfully submits that the Final Office Action in the last paragraph on page 5 and the first paragraph on page 6 addresses prefetches but does not address any queuing of a prefetch operation or any performing of a queued prefetch operation in response to a miss.

For at least the above reasons, Applicant therefore respectfully submits claims 111 and 141 are patentable over Cohn.

Claim 130

Claim 130 depends from independent claim 126 and refers to performing one or more queued operations as comprising performing a prefetch operation.

Applicant respectfully submits Cohn did not teach or suggest such feature(s) as claimed.

Applicant also respectfully submits that the Final Office Action in the last paragraph on page 5 and the first paragraph on page 6 addresses prefetches but does not address any queuing of a prefetch operation or any performing of a queued prefetch operation in response to a miss.

For at least the above reasons, Applicant therefore respectfully submits claim 130 is patentable over Cohn.

Claims 112-114, 119-121, 131-133, and 142-144

Claims 112-114, 119-121, 131-133, and 142-144 depend from independent claim 107, 126, or 137. Applicant respectfully submits these claims are patentable over Cohn because Cohn did not teach or suggest features of independent claims 107, 126, and 137 as explained above.

3. Whether claims 116-117, 135-136, and 146-147 are unpatentable under § 103(a) over Cohn and TDB.

Claims 116-117, 135-136, and 146-147

Claims 116-117, 135-136, and 146-147 depend from independent claim 107, 126, or 137. Applicant respectfully submits these claims are patentable over Cohn and TDB because Cohn did not teach or suggest features of independent claims 107, 126, and 137 as explained above.

For at least the above reasons, Applicant respectfully submits that claims 107, 109-110, 115, 118, 122-126, 128-129, 134, 137, 139-140, 145, and 148 are not anticipated under 35 U.S.C. § 102(b) by Cohn, that claims 111-114, 119-121, 130-133, and 141-144 are not unpatentable under 35 U.S.C. § 103(a) over Cohn, and that claims 116-117, 135-136, and 146-147 are not unpatentable under 35 U.S.C. § 103(a) over Cohn in view of TDB. Applicant therefore respectfully requests reversal of the rejections of claims 107, 109-126, 128-137, and 139-148.

Respectfully submitted,

Date: December 31, 2006

/Matthew C. Fagan, Reg. No. 37,542/

Matthew C. Fagan
Registration No. 37,542
Telephone: (512) 732-3936
Facsimile: (512) 732-3912 (please call first)

c/o Blakely, Sokoloff, Taylor & Zafman, L.L.P.
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025
Telephone: (503) 439-8778
Telephone: (310) 207-3800

viii. *Claims Appendix*

107. An apparatus comprising:

non-volatile cache memory; and

a controller to control access to a rotating storage device in response to requests, the controller to spin down the rotating storage device, to queue one or more operations for the rotating storage device, to spin up the rotating storage device to perform a read operation for a read request in response to a miss in non-volatile cache memory for the read request, and to perform one or more queued operations for the rotating storage device in response to the miss,

wherein the controller is to queue one or more operations for the rotating storage device while the rotating storage device is spun down.

109. The apparatus of claim 107, wherein the controller is to spin down the rotating storage device after performance of the read operation and one or more queued operations.

110. The apparatus of claim 107, wherein queued operation(s) for the rotating storage device comprise a write operation.

111. The apparatus of claim 107, wherein queued operation(s) for the rotating storage device comprise a prefetch operation.

112. The apparatus of claim 107, wherein the controller is to determine if prefetch is desirable in response to the read request and is to perform a prefetch if prefetch is desirable.

113. The apparatus of claim 107, wherein the controller is to determine if the read request is for a sequential stream and is to perform a prefetch if the read request is for a sequential stream.

114. The apparatus of claim 107, wherein the controller is to determine if one or more queued operations for the rotating storage device are desirable.

115. The apparatus of claim 107, wherein the controller is to perform one or more queued operations for the rotating storage device after the read operation.

116. The apparatus of claim 107, wherein the non-volatile cache memory comprises ferroelectric memory.

117. The apparatus of claim 107, wherein the non-volatile cache memory comprises polymer memory.

118. The apparatus of claim 107, wherein the controller comprises software.

119. The apparatus of claim 107, comprising a general-purpose processor, wherein the controller comprises software comprising a driver for execution by the general-purpose processor.

120. The apparatus of claim 107, wherein the controller comprises software for execution on a host processor.

121. The apparatus of claim 107, wherein the controller comprises a hardware controller device.

122. The apparatus of claim 107, wherein the controller comprises a digital signal processor.

123. The apparatus of claim 107, wherein the controller comprises an application specific integrated circuit.

124. The apparatus of claim 107, wherein the controller resides coincident with non-volatile cache memory.

125. The apparatus of claim 107, wherein the memory controller resides separately from both non-volatile cache memory and the rotating storage device.

126. A method comprising:

spinning down a rotating storage device;

queuing one or more operations for the rotating storage device, wherein queuing one or more operations for the rotating storage device comprises queuing one or more operations while the rotating storage device is spun down; and

in response to a miss in non-volatile cache memory for a read request, spinning up the rotating storage device and performing a read operation for the read request and one or more queued operations for the rotating storage device.

128. The method of claim 126, comprising spinning down the rotating storage device after performing the read operation and one or more queued operations.

129. The method of claim 126, wherein performing one or more queued operations for the rotating storage device comprises performing a write operation.

130. The method of claim 126, wherein performing one or more queued operations for the rotating storage device comprises performing a prefetch operation.

131. The method of claim 126, comprising determining if prefetch is desirable in response to the read request and performing a prefetch if prefetch is desirable.

132. The method of claim 126, comprising determining if the read request is for a sequential stream and performing a prefetch if the read request is for a sequential stream.

133. The method of claim 126, comprising determining if one or more queued operations for the rotating storage device are desirable.

134. The method of claim 126, comprising performing one or more queued operations for the rotating storage device after the read operation.

135. The method of claim 126, wherein the non-volatile cache memory comprises ferroelectric memory.

136. The method of claim 126, wherein the non-volatile cache memory comprises polymer memory.

137. A system comprising:

a hard disk drive;

non-volatile cache memory; and

a controller to control access to the hard disk drive in response to requests, the controller to spin down the hard disk drive, to queue one or more disk operations, to spin up the hard disk drive to perform a disk read operation for a read request in response to a miss in non-volatile

cache memory for the read request, and to perform one or more queued disk operations in response to the miss,

wherein the controller is to queue one or more disk operations while the hard disk drive is spun down.

139. The system of claim 137, wherein the controller is to spin down the hard disk drive after performance of the disk read operation and one or more queued disk operations.

140. The system of claim 137, wherein queued disk operation(s) comprise a disk write operation.

141. The system of claim 137, wherein queued disk operation(s) comprise a prefetch operation.

142. The system of claim 137, wherein the controller is to determine if prefetch is desirable in response to the read request and is to perform a prefetch if prefetch is desirable.

143. The system of claim 137, wherein the controller is to determine if the read request is for a sequential stream and is to perform a prefetch if the read request is for a sequential stream.

144. The system of claim 137, wherein the controller is to determine if one or more queued disk operations are desirable.

145. The system of claim 137, wherein the controller is to perform one or more queued disk operations after the disk read operation.

146. The system of claim 137, wherein the non-volatile cache memory comprises ferroelectric memory.

147. The system of claim 137, wherein the non-volatile cache memory comprises polymer memory.

148. The system of claim 137, wherein the system comprises a personal computer, a server, a workstation, a router, a switch, a network appliance, a handheld computer, an instant messaging device, a pager, or a mobile telephone.

ix. *Evidence Appendix*

None.

x. *Related Proceedings Appendix*

None.